AF/2825
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/678,175
Filing Date	September 28, 2000
First Named Inventor	Victor Konrad
Art Unit	2825
Examiner Name	Yelena Rossoshek
Total Number of Pages in This Submission	27
Attorney Docket Number	42390P9573

ENCLOSURES ***(check all that apply)***

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
  - ☐ PTO/SB/08
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Basic Filing Fee
  - ☐ Declaration/POA
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Steven Laut, Reg. No. 47,736 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	October 28, 2005

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Jean Svoboda		
Signature		Date	October 28, 2005

Based on PTO/SB/21 (04-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 06/04/2004.
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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 0.00

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

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☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

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FEE CALCULATION

1. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	30	- 36** =	0	X	50.00	=	$0.00
Independent Claims	6	- 6** =	0	X	200.00	=	$0.00
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple Dependent claim, if not paid
1204	300	2204	150	**Reissue independent claims over original patent
1205	300	2205	150	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (1) ($) 0.00

***or number previously paid, if greater, For Reissues, see below*

2. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify)					

SUBTOTAL (2) ($)

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Steven Laut	Registration No. (Attorney/Agent)	47,736	Telephone	(310) 207-3800
Signature				Date	10/28/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Attorney Docket No. 042390.P9573

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Patent Application of:

Victor Konrad, Vivek Joshi

Serial No. 09,678,175

Filed: September 28, 2000

For: **METHOD TO REDUCE THE POWER CONSUMPTION OF LARGE PLAS BY CLOCK GATING GUIDED BY RECURSIVE SHANNON DECOMPOSITION OF THE AND-PLANE**

Examiner: Yelena Rossoshek

Art Unit: 2825

AMENDED APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
Post Office Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Applicant submits, the following Amended Appeal Brief pursuant to 37 C.F.R. § 41.37 for consideration by the Board of Patent Appeals and Interferences. Applicant has submitted payment with the Appeal Brief submitted on August 1, 2005 in the amount of $500.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 41.20(b)(2). This brief does not include any new or non-admitted amendments or any new or non-admitted affidavit or other evidence.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16, 1.17 or 41.29(b)(2), particularly extension of time fees.

I. REAL PARTY IN INTEREST

Victor Konrad and Vivek Joshi, the parties named in the caption, assigned their rights to that disclosed in the subject application through an assignment recorded on September 28, 2000 (011220/0553) to Intel Corporation of Santa Clara, California. Thus, as owner at the time the brief is being filed, Intel Corporation of Santa Clara, California, is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-3, 6, 7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39 are pending in the present application. Claims 1-3, 6, 7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39 are rejected. Claims 1-3, 6, 7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39 are being appealed.

IV. STATUS OF AMENDMENTS

Applicant has not amended the claims subsequent to a final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Applicant submits below a concise explanation of the subject matter defined in independent claims 1, 10, 17, 24, 29 and 36.

Applicant's claim 1 defines a method for using a splitting variable to efficiently reduce power consumption and control power in large PLAs. Applicant's method determines an optimum splitting variable for dividing a programmable logic array (PLA) into at least two sub-PLAs (Specification, page 6, lines 4-13) by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA (Specification, page 13, line 8 – page 14, line 4). A column is selected with the smallest overhead (Specification, page 13, lines 26-29) in the AND plane of the set of equations

representing the PLA.

Each sub-PLA of the two sub-PLAs have an AND plane and an OR plane (Specification, page 4, lines 8-10). A first sub-PLA includes products where the splitting variable is in complemented form (Specification, page 6, lines 13-14). A second sub-PLA includes products where the splitting variable is in uncomplemented form (Specification, page 6, lines 15-16). The splitting variable corresponds to a specific input, output and product in the set of equations representing the PLA.

A set of equations representing a PLA are divided into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable (Specification, page 6, lines 18-20; Tables 1 and 2). A topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA (Fig. 3) are determined.

Gating logic is applied to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA (Specification, page 7, lines 6-8). Power consumption is controlled in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption (Specification, page 8, lines 21-24). An OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA (Specification, page 8, lines 8-9).

Applicant's claim 10 defines a method for using a splitting variable to efficiently reduce power consumption and control power in large PLAs. This embodiment differs from the embodiment asserted in claim 1 by the following. Outputs of the equations representing the at least two sub-PLAs are merged (Specification, page 6, lines 16-17). An OR plane of the topological circuit representation of a first sub-PLA is either interleaved (Fig. 2) or separated with an OR plane of the topological circuit representation of a second sub-PLA (Fig. 3).

Applicant's claim 17 defines a program storage device readable by a machine including instructions that cause the machine to perform similar actions according to claim 1 (see above discussion relating to claim 1; specification, page 15, lines 9-14).

Applicant's claim 24 defines a program storage device readable by a machine including instructions that cause the machine to perform similar actions according to claim 10 (see above discussion relating to claim 10; specification, page 15, lines 9-14).

Applicant's claim 29 defines a method for using a splitting variable to efficiently reduce power consumption and control power in large PLAs. This embodiment differs from the embodiment asserted in claim 1 by an OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA (Fig. 2).

Applicant's claim 36 defines a method for using a splitting variable to efficiently reduce power consumption and control power in large PLAs. This embodiment differs from the embodiment asserted in claim 1 by an OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA (Fig. 2).

Applicant's claim 36 defines a program storage device readable by a machine including instructions that cause the machine to perform similar actions according to claim 29 (see above discussion relating to claim 29; specification, page 15, lines 9-14).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-3, 6, 7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39 are anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 6,492,835 issued to Shau ("Shau"). Applicant presents this ground of rejection for review.

VII. ARGUMENT

A. It is asserted in the Office Action that Claims 1-3, 6, 7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39 are rejected under 35 U.S.C. §102(b) as being anticipated by Shau. The following discussion sets forth in detail Applicant's analysis with respect to the patentability of claims 1, 1-3, 6, 7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39.

According to MPEP §2131,

> '[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

1. Claims 1-3, 6, 7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39

Applicant's amended independent claim 1 contains the limitations of

> ...determining an optimum splitting variable for dividing a programmable logic array (PLA) into at least two sub-PLAs by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub- PLAs includes products in

which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; dividing a set of equations representing a PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA.

Applicant's amended independent claim 10 contains the limitations of

determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing at least two sub-PLAs by avoiding unbalanced columns in an AND plane of the equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the equations representing the PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; dividing the set of equations representing the PLA into equations representing the at least two sub-PLAs; merging outputs of the equations representing the at least two sub-PLAs; determining a topological circuit representation of the equations representing the at least two sub-PLAs;

applying gating logic to the topological circuit representation of the at least two sub-PLAs; and controlling power consumption in the topological representation of the at least two sub-PLAs so only one of the at least two sub-PLAs contributes to power consumption, wherein an OR

plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA.

Applicant's amended independent claim 17 contains the limitations of

determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, said first sub-PLA and said second sub-PLA each have an AND plane and an OR plane, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; divide the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determine a topological circuit representation of first sub-PLA and the second sub-PLA; apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein the topological circuit representation an OR plane of the first sub-PLA is interleaved with an OR plane of the second sub-PLA.

Applicant's amended independent claim 24 contains the limitations of

determine an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing at least two sub-PLAs by avoiding unbalanced columns in an AND plane of the equations representing the sub-PLA and selecting a column with smallest overhead in the AND plane of the equations representing the sub-PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input,

output and product in the set of equations representing the PLA; divide the set of equations representing the PLA into equations representing the at least two sub-PLAs; merge outputs of the equations representing the at least two sub-PLAs; determine a topological circuit representation of the equations representing the at least two sub-PLAs; apply gating logic to the topological circuit representation of the at least two sub-PLAs; and control power consumption in the topological circuit representation of the at least two sub-PLAs so only one of the at least two sub-PLAs contributes to power consumption, wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA.

Applicant's amended independent claim 29 contains the limitations of

determining an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an AND plane and an OR plane by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA; dividing the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein an OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA.

Applicant's amended independent claim 36 contains the limitations of

> determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an AND plane and an OR plane by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA; divide a set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determine a topological circuit representation of the first sub-PLA and the second sub-PLA; apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein in the topological circuit representation an OR plane of the first sub-PLA is separated from an OR plane of the second sub-PLA.

It is asserted in the Office Action that Shau teaches "determining an optimum splitting variable for dividing a programmable logic array (PLA)" based on the disclosure at column 4, lines 31-33. This portion of Shau, however, does not teach, disclose or suggest a "splitting variable." Shau does disclose optimization methods, but not by using an optimum splitting variable. Shau teaches using minterm sorting procedures, before a PLA is split into sub-PLAs (see Shau, column 7, line 15 to column 8, line 26). Applicant notes that a minterm is defined by Shau as "[t]he horizontal lines of the AND array and OR array represent intermediate logic terms called 'minterms' in the art." (Shau, column 2, lines 13-15). An ordinary person skilled in the art would differentiate "logic terms" with a variable (i.e., splitting variable). Nowhere in Shau is it taught, disclosed or suggested "determining an optimum splitting variable for dividing a programmable logic array (PLA) into at least two sub-PLAs by avoiding unbalanced

columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA." This is distinguishable from Shau as Shau discloses balancing minterms of sub-PLAs and organizing sub-PLAs after they are formed (i.e., after the PLA is split), even by adding "dummy minterms." (Shau, column 8, lines 40-41).

Moreover, Shau asserts that there are many other methods applicable to partition a large PLA into sub-PLA's, but none of the teachings of Shau disclose, teach, or suggest all the limitations contained in Applicant's claims 1, 10, 17, 24, 29 and 36. (See Shau, column 8, lines 32-47). Shau, just by mentioning other methods can be used for partitioning a large PLA into sub-PLAs does not make all other methods become anticipated by Shau. Applicant notes that while Shau is concerned with power savings for PLAs, and asserts sub-PLAs and balancing minterms, nowhere in Shau is Shannon decomposition mentioned for which Applicant's splitting variable is determined.

Therefore, since Shau does not disclose, teach or suggest all of Applicant's amended claims 1, 10, 17, 24, 29 and 36 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Shau. Thus, Applicant's amended claims 1, 10, 17, 24, 29 and 36 are not anticipated by Shau. Additionally, the claims that directly or indirectly depend on claims 1, 10, 17, 24, 29 and 36, namely claims 2-3 and 6-9, 11-16, 18-19 and 22-23, 25-28, 30-35, and 37-40, respectively, are also not anticipated by Shau for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(b) rejections for claims 1-3, 6, 7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39 are respectfully requested.

CONCLUSION

Based on the foregoing, Applicant requests that the Board overturn the rejection of all pending claims and hold that all of the claims of the present application are allowable.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: October 28, 2005

By: _____
Steven Laut, Reg. No. 47,736

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I hereby certify that this correspondence is being deposited as First Class Mail, with sufficient postage, with the United States Postal Service in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on October 28, 2005.

_____
Jean Svoboda

VIII. CLAIMS APPENDIX

The claims involved in this Appeal are as follows:

Claim 1 (Previously Presented): A method comprising:

determining an optimum splitting variable for dividing a programmable logic array (PLA) into at least two sub-PLAs by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA;

dividing a set of equations representing a PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA;

applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and

controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA.

Claim 2 (Original): The method of claim 1, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 3 (Original): The method of claim 1, further comprising merging an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein merging the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA forms a logical equivalent of the PLA.

Claims 4-5 (Canceled)

Claim 6 (Original): The method of claim 1, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

Claim 7 (Original): The method of claim 1, further comprising delaying a clock to an OR plane of one of the topological circuit representation of the first sub-PLA and the topological circuit representation of the second sub-PLA.

Claim 8 (Canceled)

Claim 9 (Original): The method of claim 1, wherein determining a topological circuit representation of first sub-PLA and the second sub-PLA is created by computer aided design.

Claim 10 (Previously Presented): A method comprising:

determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing at least two sub-PLAs by avoiding unbalanced columns in an AND plane of the equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the equations representing the PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs

includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA;

dividing the set of equations representing the PLA into equations representing the at least two sub-PLAs;

merging outputs of the equations representing the at least two sub-PLAs;

determining a topological circuit representation of the equations representing the at least two sub-PLAs;

applying gating logic to the topological circuit representation of the at least two sub-PLAs; and

controlling power consumption in the topological representation of the at least two sub-PLAs so only one of the at least two sub-PLAs contributes to power consumption,

wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA.

Claim 11 (Original): The method of claim 10, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 12 (Original): The method of claim 10, wherein the equations representing the plurality of sub-PLAs are divided recursively based on a determined optimum splitting variable for each equation representing a sub-PLA.

Claim 13 (Original): The method of claim 12, wherein each product of the equations representing the plurality of sub-PLAs is obtained by omitting literals in the equations representing the PLA.

Claim 14 (Original): The method of claim 13, wherein a product of the omitted literals is used in the topological circuit representation of the plurality of sub-PLAs to gate a clock of each product of the plurality of sub-PLAs.

Claim 15 (Canceled)

Claim 16 (Original): The method of claim 12, wherein the step of determining the optimum splitting variable for each of the equations representing the sub-PLA further comprises avoiding unbalanced columns in an AND plane of the equations representing the sub-PLA; and selecting a column with smallest overhead in the AND plane of the equations representing the sub-PLA.

Claim 17 (Previously Presented): A program storage device readable by a machine comprising instructions that cause the machine to:

determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, said first sub-PLA and said second sub-PLA each have an AND plane and an OR plane, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA;

divide the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determine a topological circuit representation of first sub-PLA and the second sub-PLA;

apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and

control power consumption in the topological circuit representation of the first

sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption,
wherein the topological circuit representation an OR plane of the first sub-PLA is interleaved with an OR plane of the second sub-PLA.

Claim 18 (Original):The program storage device of claim 17, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 19 (Original):The program storage device of claim 17, further comprising instructions that cause the machine to merge an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein the instruction that causes the machine to merge the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA, forms a logical equivalent of the equations representing the PLA.

Claims 20-21 (Cancelled)

Claim 22 (Original):The program storage device of claim 17, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

Claim 23 (Canceled)

Claim 24 (Previously Presented): A program storage device readable by a machine comprising instructions that cause the machine to:

determine an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing at least two sub-PLAs by avoiding unbalanced columns in an AND plane of the equations representing the sub-PLA and selecting a column with smallest overhead in the AND plane of the equations representing the sub-PLA, each sub-PLA of said at least two sub-

PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA;

divide the set of equations representing the PLA into equations representing the at least two sub-PLAs;

merge outputs of the equations representing the at least two sub-PLAs;

determine a topological circuit representation of the equations representing the at least two sub-PLAs;

apply gating logic to the topological circuit representation of the at least two sub-PLAs; and

control power consumption in the topological circuit representation of the at least two sub-PLAs so only one of the at least two sub-PLAs contributes to power consumption,

wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA.

Claim 25 (Original): The program storage device of claim 24, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 26 (Original): The program storage device of claim 24, wherein the instruction causing the machine to divide the equations representing the plurality of sub-PLAs divides recursively based on a determined optimum splitting variable for each equation representing a sub-PLA.

Claim 27 (Original): The program storage device of claim 24, wherein the instruction causing the machine to determine the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the equations representing the PLA; and

selecting a column with smallest overhead in the AND plane of the equations representing the PLA.

Claim 28 (Canceled)

Claim 29 (Previously Presented): A method comprising:

determining an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an AND plane and an OR plane by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA;

dividing the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA;

applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein an OR plane of the topological circuit representation of the first sub-PLA is

separated from an OR plane of the topological circuit representation of the second sub-PLA.

Claim 30 (Previously Presented): The method of claim 29, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 31 (Previously Presented): The method of claim 29, further comprising merging an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein merging the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA forms a logical equivalent of the PLA.

Claim 32 (Previously Presented): The method of claim 29, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

Claim 33 (Previously Presented): The method of claim 29, further comprising delaying a clock to an OR plane of one of the topological circuit representation of the first sub-PLA and the topological circuit representation of the second sub-PLA.

Claim 34 (Canceled)

Claim 35 (Previously Presented): The method of claim 29, wherein determining a topological circuit representation of first sub-PLA and the second sub-PLA is created by computer aided design.

Claim 36 (Previously Presented): A program storage device readable by a machine comprising instructions that cause the machine to:

determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said

second sub-PLA each having an AND plane and an OR plane by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA;

divide a set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determine a topological circuit representation of the first sub-PLA and the second sub-PLA;

apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and

control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein in the topological circuit representation an OR plane of the first sub-PLA is separated from an OR plane of the second sub-PLA.

Claim 37 (Previously Presented): The program storage device of claim 36, wherein the PLA to be divided is partially optimized by computer aided design.

Claim 38 (Previously Presented): The program storage device of claim 36, further comprising instructions that cause the machine to merge an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA,

wherein the instruction that causes the machine to merge the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA, forms a logical equivalent of the equations representing the PLA.

39. (Previously Presented) The program storage device of claim 36, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

Claim 40 (Canceled)

IX. EVIDENCE APPENDIX

Applicant does not submit further evidence as the evidence relied on for the grounds of rejection pertain only to the cited prior art.

X. RELATED PROCEEDINGS APPENDIX

Applicant asserts there are no related proceedings that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.